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Appl. No. 10/827,389  
Reply to Final Office Action of October 20, 2006

### REMARKS

Claims 1, 2, 4-5 and 7-15 are pending in the subject application. Claims 1, 7-11 and 14 are amended. Claim 30 is newly added. Claims 8 and 13 were previously withdrawn. Reconsideration of this application and allowance of each of pending claims 1, 2, 4-5, 7, 9-12, 14, 15 and 30 are respectfully requested.

### Claims Rejections under 35 U.S.C. §103(a)

The Action rejects Claims 1, 2, 4-5, 7, 9-12, 14 and 15 under 35 U.S.C. §103(a), for allegedly being obvious over the applicant's admitted prior art (AAPA) of the present application in combination with U.S. Patent Publication No. 2003/0095427 to Afghahi et al. ("Afghahi") and to U.S. Patent Publication No. 2004/0043587 to Lawlor ("Lawlor").

Claim 1 has been amended to recite:

A single transistor random access memory cell, comprising:  
a transfer gate over a substrate having a recess;  
a storage capacitor having a capacitor plate horizontally adjacent to the transfer gate; and  
a shallow trench isolation, STI, insulator within the recess of the substrate, the STI insulator having a height smaller than a depth of the recess of the substrate, wherein the capacitor plate covers the STI insulator and conformially covers a sidewall of the recess of the substrate. (Emphasis added).

Supports for the amendments can be found at, for example, Paragraphs [0022]-[0037] and FIGS. 2A-2C. No new matter is added. Claims 7-11 and 14 are amended in consistency with the amendments of Claim 1. The amended Claim 1 is not obvious over the art of record in view of the foregoing amendments and following arguments.

AAPA discloses a traditional dynamical random access memory (DRAM) cell. STI structure 110 is formed within the recess (not labeled) of substrate 100. (Paragraph [0006]). In FIG. 1 of AAPA, substrate 100 having STI structure 110 formed therein has a planar surface under transfer gate 120 and electrode plate 130. Clearly, the height of STI structure 110 is equal to the depth of the recess of substrate 100. Further, electrode plate 130 only covers STI structure 110, and does not cover a sidewall of the recess of substrate 100. Therefore, AAPA fails to

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teach or suggest that the STI insulator has a height smaller than a depth of the recess of the substrate and that the capacitor plate covers the STI insulator and conformally covers a sidewall of the recess of the substrate.

Afghahi discloses a DRAM cell which includes native device 16, i.e., transistor, for charge storage. Native device 16 includes substrate 18 doped with p-type material defining a surface 19. Gate 28 is over surface 19 and sections 20, 24 and 26 of substrate 18 are doped with different types of material. (Paragraph [0011] and FIG. 3). **Nothing** in Afghahi's description or drawings shows a **STI structure**. Accordingly, Afghahi fails to teach or suggest that the STI insulator has a height smaller than a depth of the recess of the substrate and that the capacitor plate covers the STI insulator and conformally covers a sidewall of the recess of the substrate.

Lawlor is directed to a method for improving conductivity at an **interface between a polysilicon layer and a conductive layer** in an integrated circuit device. (Paragraph [0002]). Substrate 30 includes N+ doped regions 32A, 32B and 32C. (Paragraph [0020]). Gate dielectric layer 34 is formed over **planar** substrate 30. (Paragraph [0021]). Wordline stacks are then formed over gate dielectric layer 34. (Paragraph [0022] and FIG. 3). The wordline stacks are etched into polysilicon layer 36 in a first etch and etched down to substrate 30 during a second etch. (Paragraphs [0026]-[0027] and FIG. 4). An angled implant is then used to break up nitride layer 44 between the first etch and the second etch. (Paragraph [0028] and FIG. 5). **Nothing** in Lawlor's description or drawings shows a **STI structure**. Accordingly, Lawlor fails to teach or suggest that the STI insulator has a height smaller than a depth of the recess of the substrate and that the capacitor plate covers the STI insulator and conformally covers a sidewall of the recess of the substrate.

Based on the foregoing, AAPA, Afghahi and Lawlor fail to teach or suggest that the STI insulator has a height smaller than a depth of the recess of the substrate and that the capacitor plate covers the STI insulator and conformally covers a sidewall of the recess of the substrate. Thus, a prima facie case of obviousness has not been established, and the amended Claim 1 thus would not have been obvious over the combined teachings of AAPA, Afghahi and Lawlor. Withdrawal of the rejection to Claim 1 is respectfully requested and Claim 1 is therefore allowable.

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Claims 2, 4-5, 7, 9-12, 14 and 15 depend from Claim 1 and are therefore not obvious over the art of record via virtue of their dependencies. Withdrawal of the rejections to Claims 2, 4-5, 7, 9-12, 14 and 15 are respectfully requested.

From the foregoing, reconsideration and withdrawal of the § 103 (a) rejections to Claims 1, 2, 4-5, 7, 9-12, 14 and 15 are respectfully requested.

**New Claim 30**

Claim 30 recites that the capacitor has a storage node having an MOS native device with a near zero threshold voltage to form an inversion layer, which was originally recited in Claim 1 and is now deleted from claim 1. Claim 30 depends from Claim 1 and is therefore not obvious over the art of record by virtue of dependency.

**Claims 8 and 13**

Withdrawn Claims 8 and 13 depend from Claim 1 and are in condition for rejoinder upon allowance of the amended Claim 1.

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**Conclusion**

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Early notification to that effect is respectfully requested.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

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